transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

2. (Twice Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface in a decoder circuit of a [peripheral] driver circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

3. (Twice Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface in a buffer circuit of a [peripheral] driver circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands separately.

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8. (Twice Amended) An electro-optical device comprising:

at least two transistors provided on an insulating surface in a [peripheral] driver circuit of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

REMARKS

The Official Action mailed August 4, 2000 has been received and its contents carefully noted. Claims 1-14, 16-20 and 22-70 were pending in the Official Action.

Applicants hereby elect the species of the embodiment of Figure 3, without traverse, that